

NAND Memory Array Incorporating Multiple Write Pulse Programming Of Individual Memory Cells And Method For Operation Of Same En—Hsing Chen, et al. 10/729,844

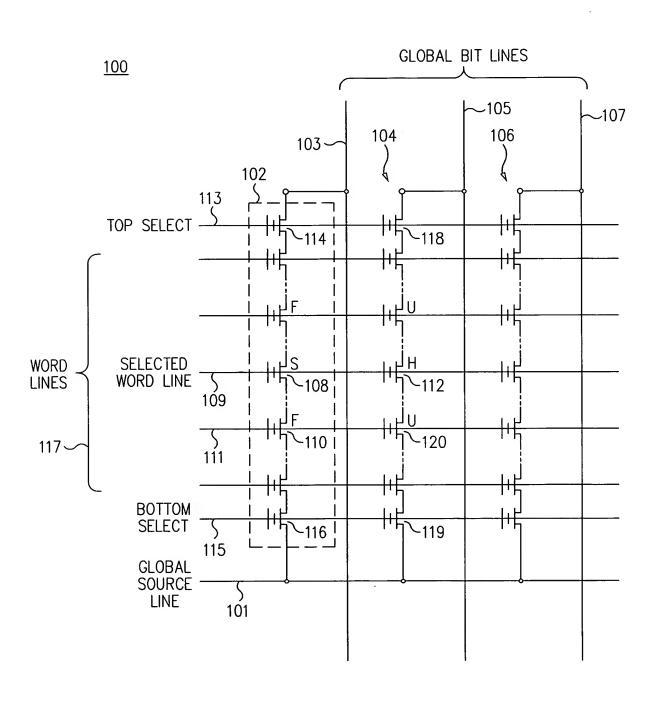
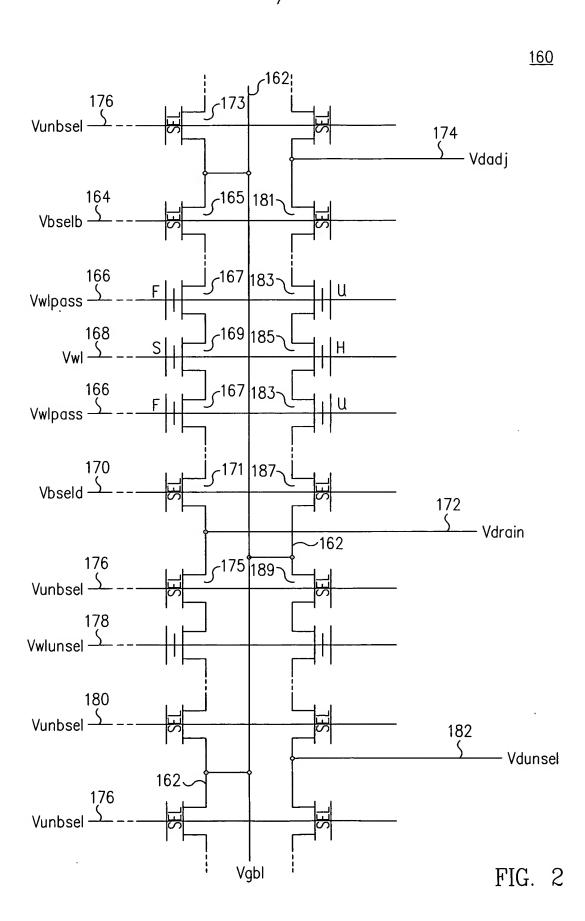


FIG. 1



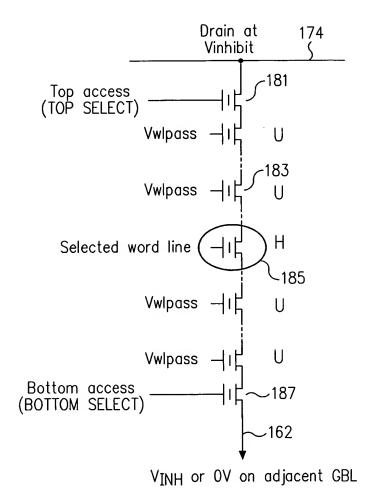
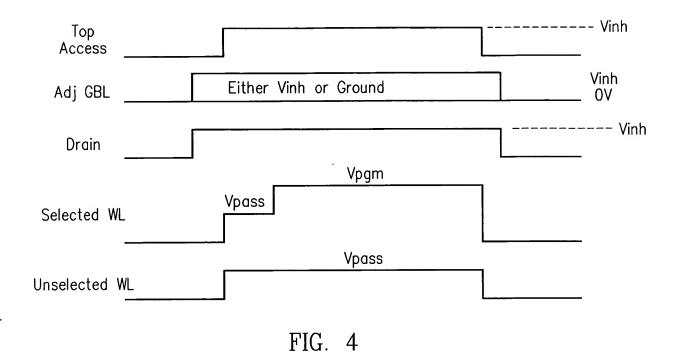


FIG. 3

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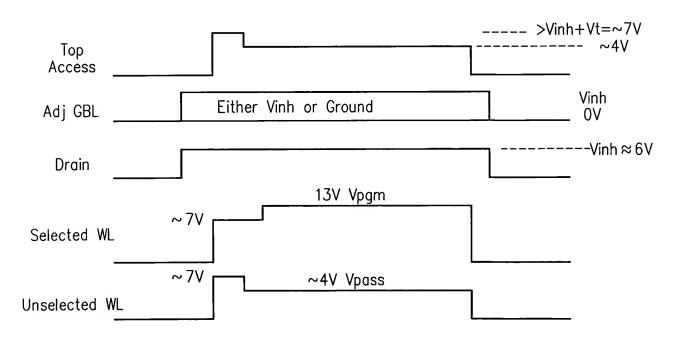
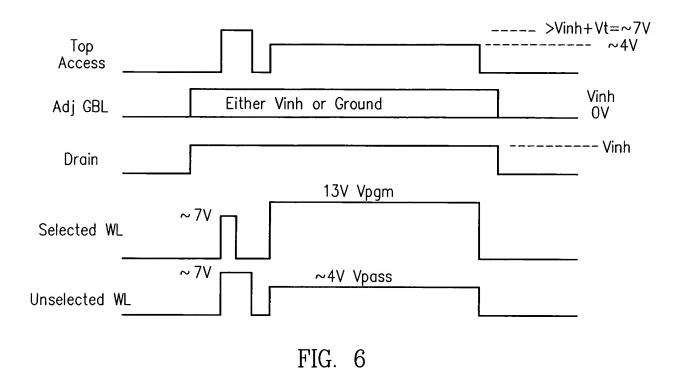


FIG. 5

NAND Memory Array Incorporating Multiple Write Pulse Programming Of Individual Memory Cells And Method For Operation Of Same En-Hsing Chen, et al. 10/729,844

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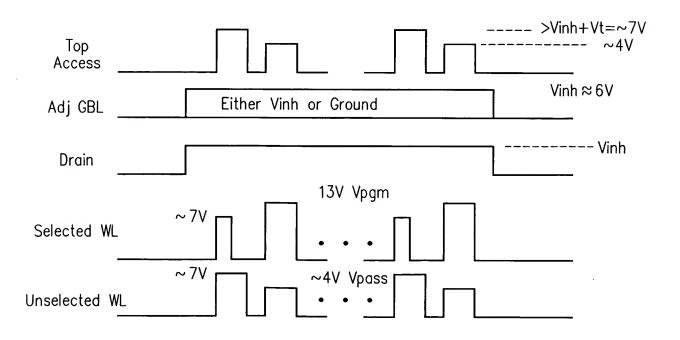
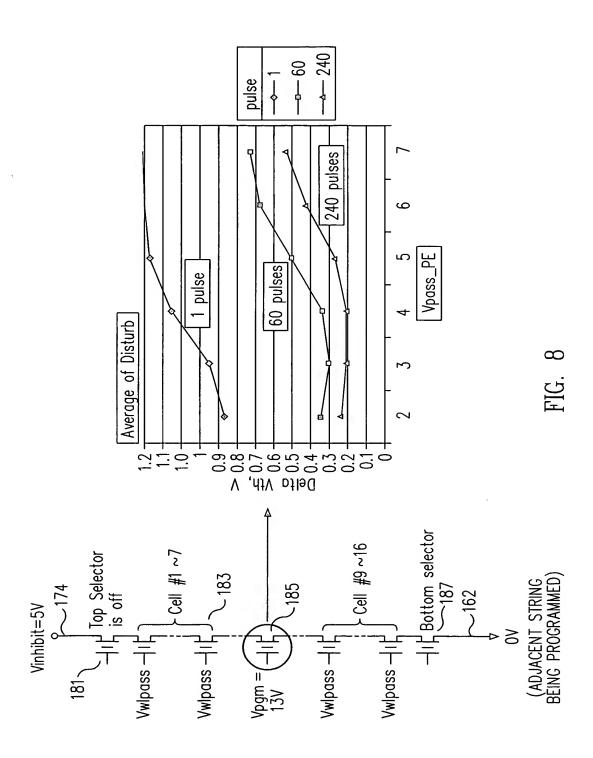
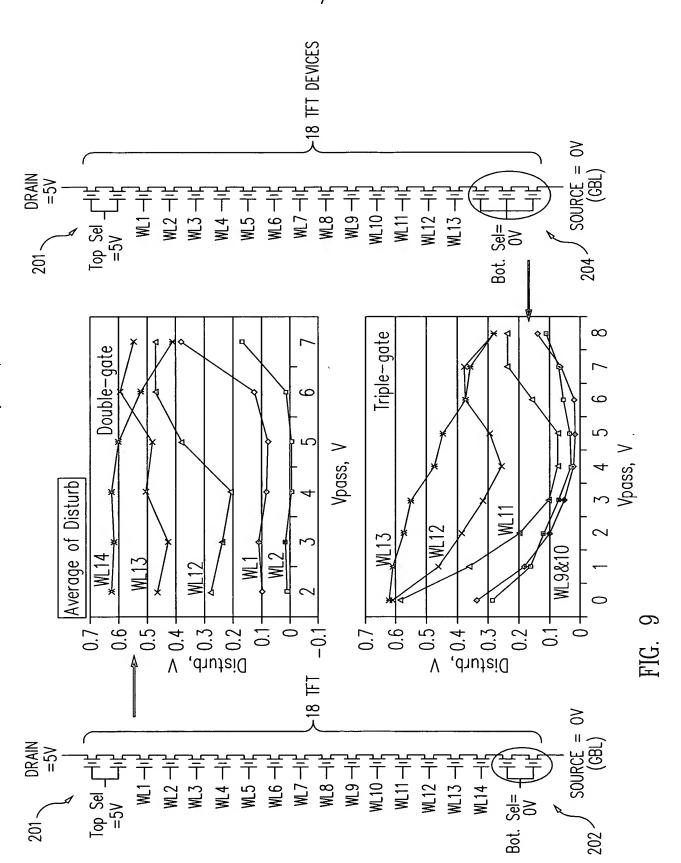
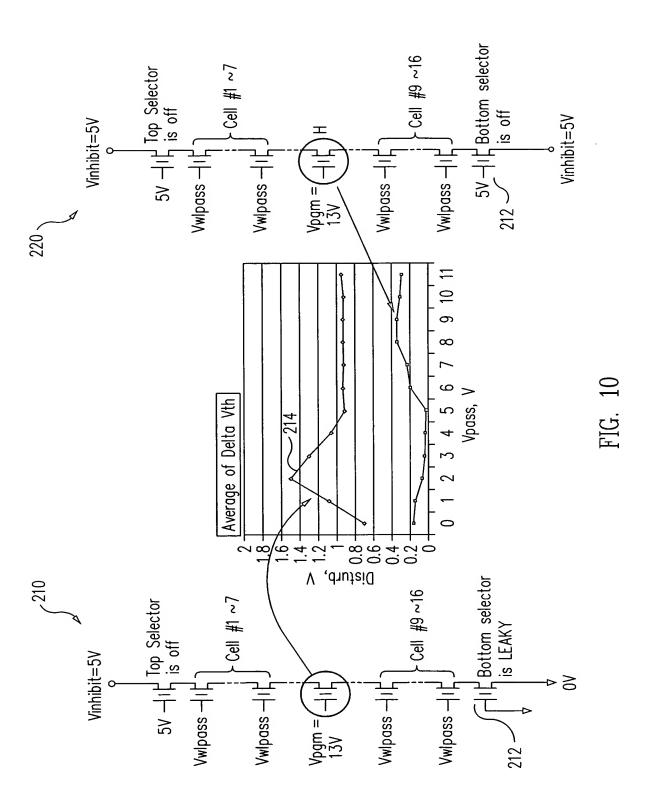
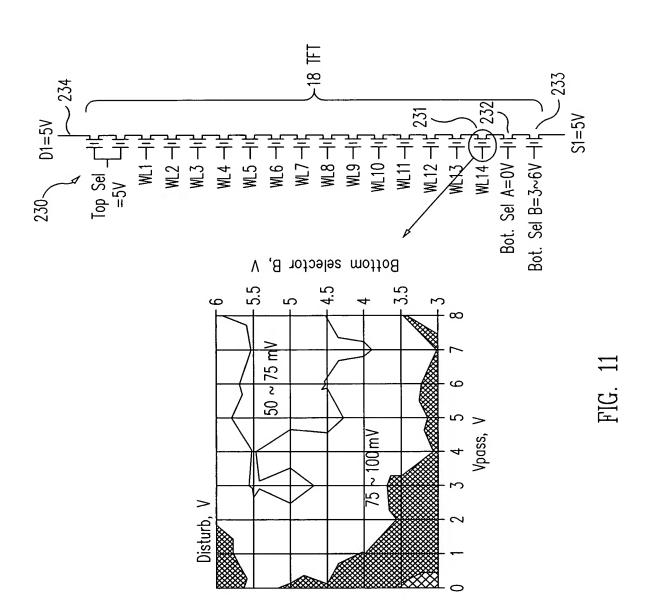


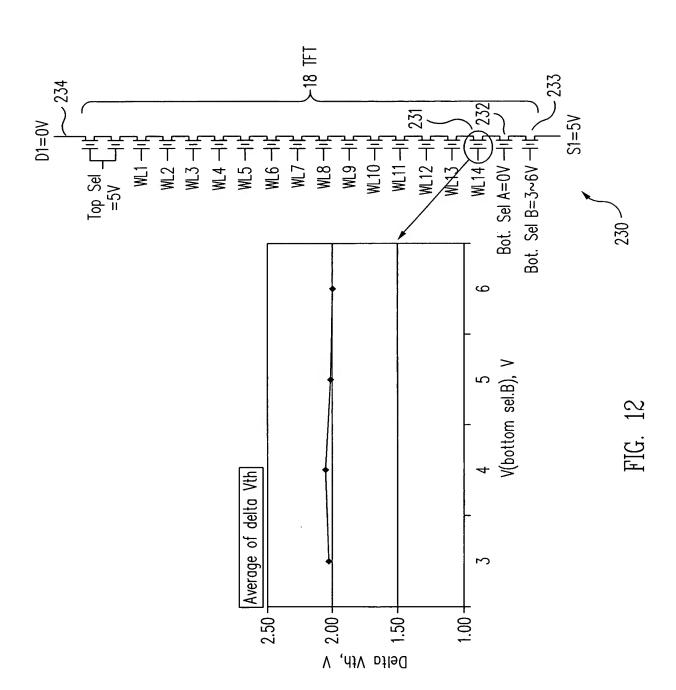
FIG. 7











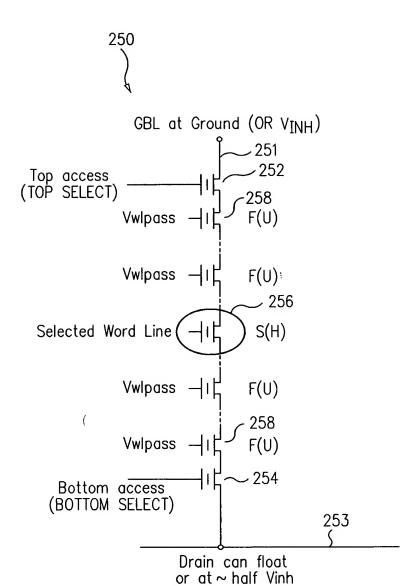
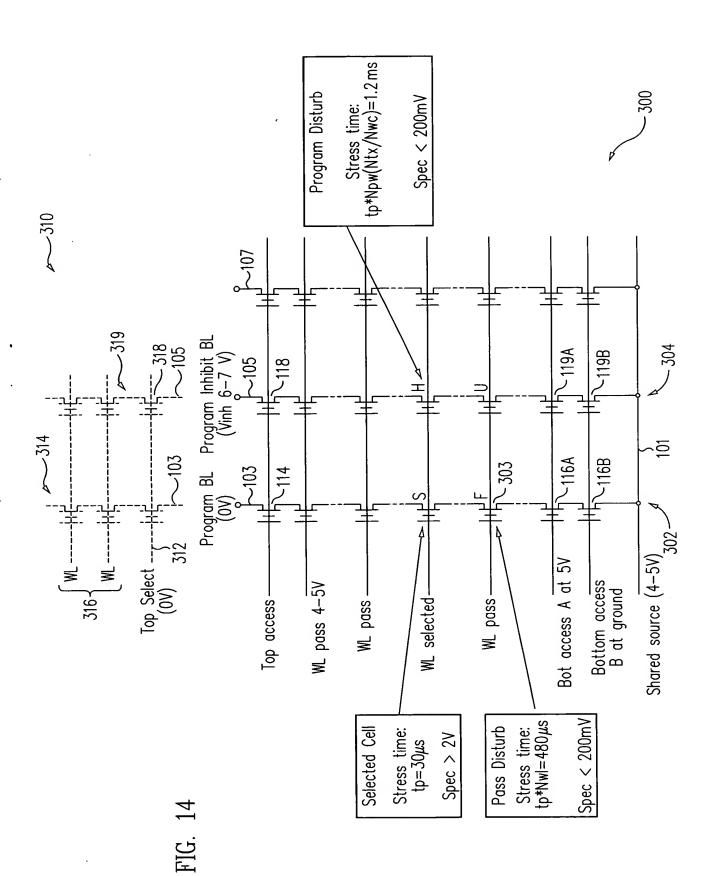


FIG. 13



NAND Memory Array Incorporating Multiple Write Pulse Programming Of Individual Memory Cells And Method For Operation Of Same En-Hsing Chen, et al. 10/729,844

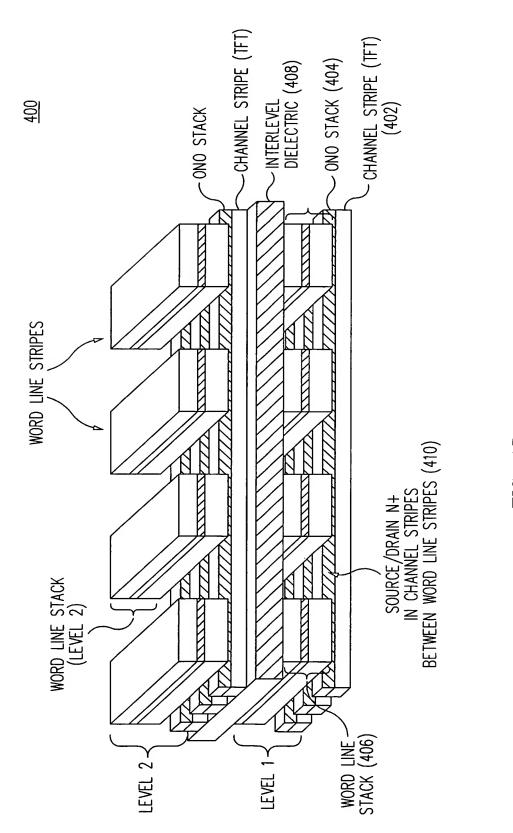


FIG. 15

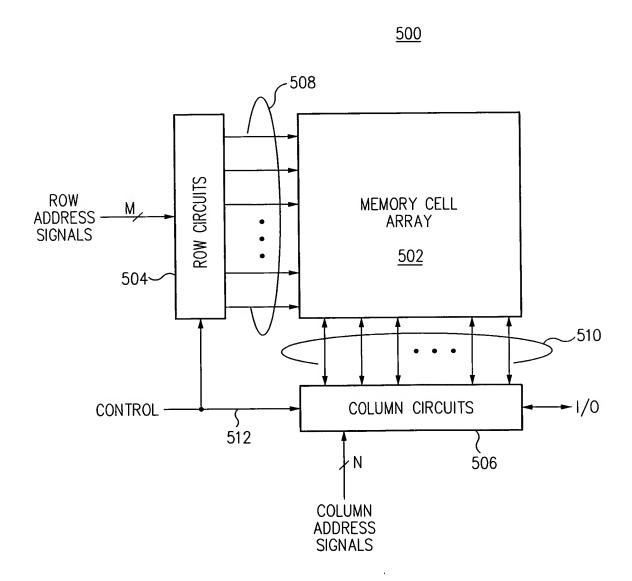
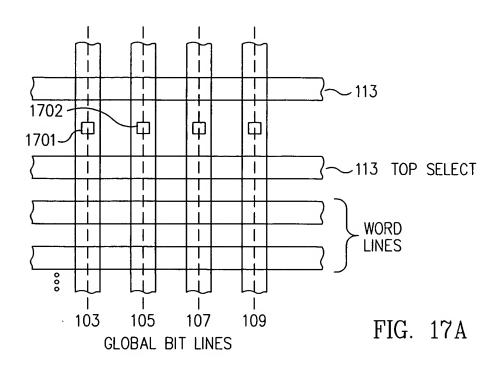


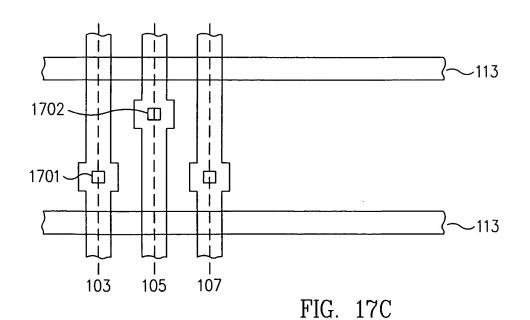
FIG. 16

NAND Memory Array Incorporating Multiple Write Pulse Programming Of Individual Memory Cells And Method For Operation Of Same En-Hsing Chen, et al. 10/729,844

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GLOBAL BIT LINES 103, 107 ON ONE LAYER > FIG.~17B GLOBAL BIT LINES 105, 109 ON 2ND LAYER > FIG.~17B



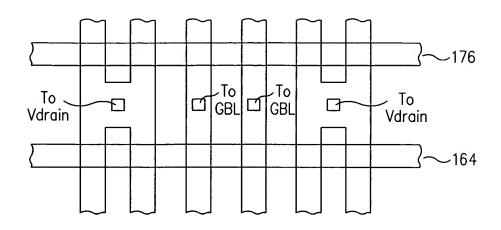
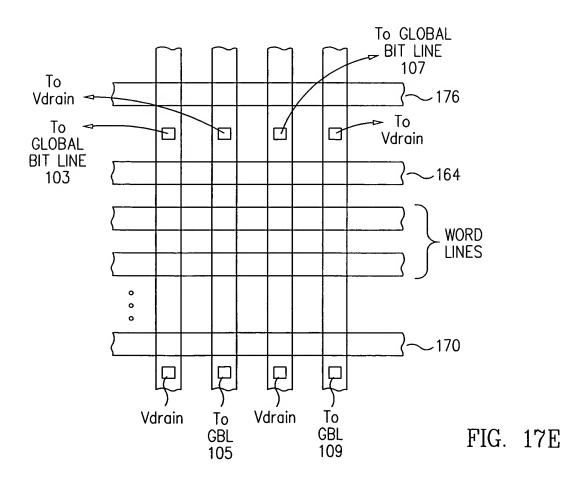


FIG. 17D



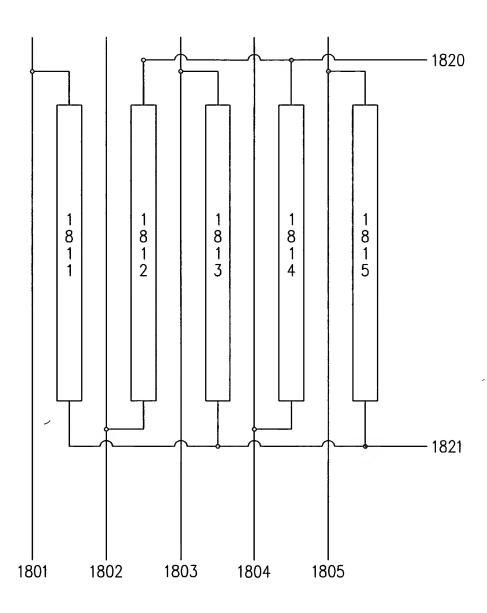


FIG. 18